`

Low-power MEMS tri-axial accelerometer digital output sensor

General description

The SGA100 is a low-power and high performance tri-axial, low-g accelerometer with digital SPI / I²C serial interface standard output, aiming for low-power consumer market applications

The Sensor allow measurement of accelerations in 3 perpendicular axes and thus senses tilt, motion, shock, and vibration handhelds, computer peripherals, Black Box and Robot vacuum.

The device features low-power operational modes that allow advanced power saving and smart sleep to wake-up functions.

The SGA100 has dynamically user selectable full scales of ±2g/±4g/±8g/±16g and it is capable of measuring accelerations with output data rates from 25Hz to 3KHz.

The SGA100 is available in small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

# KEY FEATURE

* Three-axis accelerometer
* Supply voltage, 2.0V to 3.6V
* Programmable ±2g/±4g/±8g/±16g
* Power save modes
* HPF/LPF digital filter, interrupt mode
* Calibration possibility for offset and sensitivity
* 16bit ADC resolution
* SPI/I²C Digital interface
* Sleep to wakeup function
* Low power consumption
* Capable output data rate 25Hz to 3KHz
* Support Free fall function and Motion

Detection function

Applications

* Black Box(Impact Recognition and logging )
* Shock detection
* Robot Vacuum
* Gaming Device
* Pedometer
* Display Orientation
* Digital cameras and camcorders
* Navigation devices
* Handheld devices

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1. Block Diagram and Pin Description
   1. Block Diagram



Figure 1. Block Diagram

* 1. Pin Connection And Description
     1. Pin Connection

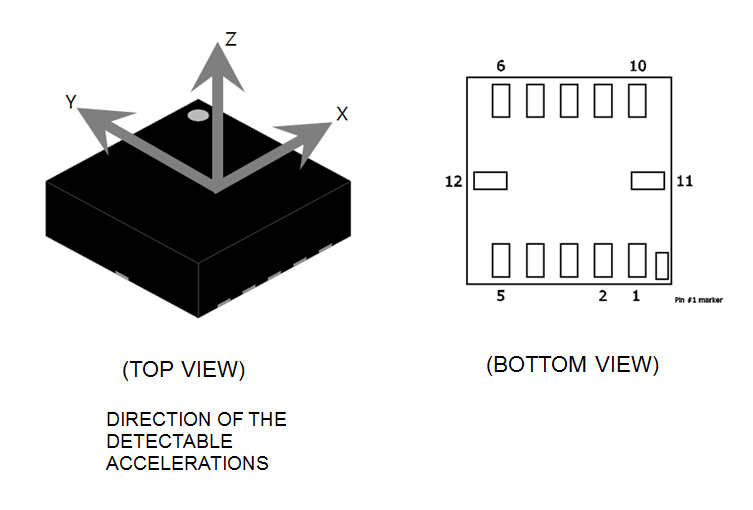


Figure 2. Pin Connection

* + 1. Pin Description

Table 1. Pin Description

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin#** | **Pin Name** | | **Description** |
| 1 | Reserved(VDDA18) | | NC(Not Connected) |
| 2 | VDDA | | Power supply 3.3V for Analog |
| 3 | GND | | Analog ground |
| 4 | INT1 | | Interrupts |
| 5 | CS | | I²C/SPI Mode Selection(1:I²C mode 0:SPI Enable) |
| 6 | SCK | SCL | I²C Serial Clock |
| SPC | SPI Serial Port Clock |
| 7 | SDO | SDO | SPI Serial Data Output |
| 8 | SDI | SDA | I²C serial data access |
| SDI | SPI Serial data Input |
| 9 | VDDIO | | Power supply 3.3V for IO Pins |
| 10 | Reserved(AID) | | NC(Not Connected) |
| 11 | Reserved(BOTM) | | NC(Not Connected) |
| 12 | Reserved(VPP) | | NC(Not Connected) |

1. Device specifications
   1. Mechanical characteristics

Typical specification is not guaranteed. VDDA=2.5v, T=25℃

Table 2. Mechanical characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameters** | **Conditions** | **Min** | **Typical** | **Max** | **Units** |
| S | Sensitivity | FS 00(±2g) |  | 16384 |  | LSB/g |
| FS 01(±4g) |  | 8192 |  |
| FS 10(±8g) |  | 4096 |  |
| FS 11(±16g) |  | 2048 |  |
| FS | Acceleration Range | FS 00 |  | ±2 |  | g |
| FS 01 |  | ±4 |  |
| FS 10 |  | ±8 |  |
| FS 11 |  | ±16 |  |
| AO | Acceleration output resolution | 2´s component |  |  | 16 | bit |
| TCS | Temperature Coefficient of Sensitivity | FS 00 |  | 0.015 | 0.02 | %/ ºC |
| TCO | Temperature Coefficient of Offset | FS 00 |  | ±0.5 | ±1 | mg/ ºC |
|
| ZO | Zero-g offset accuracy | FS 00 T=25 ºC  MSL3 |  | ±40 |  | mg |
| ND | Noise density | FS 00 T=25 ºC  ODR 50Hz |  | 250 |  | ㎍/√Hz |
| OT | Operating Temperature |  | -40 |  | 85 | ºC |
| NL | Non Linearity | FS 00 T=25 ºC |  | ±0.5 |  | %FS |
| CS | Cross Axis Sensitivity | FS 00 T=25 ºC  ODR 50Hz |  | 2 |  | % |

* The product is factory calibrated at 2.5 V.
* The operational power supply range is from 2.0V to 3.6 V.
* Zero-g offset accuracy value after MSL3 preconditioning
  1. Electrical characteristics

Typical specification is not guaranteed. VDDA=2.5v, T=25℃

Table 3. Electrical characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameters** | **Conditions** | **Min** | **Typical** | **Max** | **Units** |
| VDD | Supply voltage |  | 2.0 | 2.5 | 3.6 | V |
| VDDIO | I/O pin supply Voltage |  | 1.6 | 2.5 | 3.6 | V |
| CCN | Current Consumption in Normal mode | T=25 ºC ODR 50hz |  | 500 |  | µA |
| CCL | Current Consumption in Low-power mode | Sleep=50msec  T=25 ºC ODR 1.6khz |  | 75 |  | µA |
| CCPD | Current Consumption in Power-down mode |  |  | 2 |  | µA |
| ODR | Output Data Rate In Normal mode | DR bit Set to 000 |  | 25 |  | Hz |
| DR bit Set to 001 |  | 50 |  |
| DR bit Set to 010 |  | 100 |  |
| DR bit Set to 011 |  | 200 |  |
| DR bit Set to 100 |  | 400 |  |
| DR bit Set to 101 |  | 780 |  |
| DR bit Set to 110 |  | 1600 |  |
| DR bit Set to 111 |  | 3000 |  |
| TOT | Turn On Time | ODR max |  | 3 |  | ms |
| WUT | Wake Up Time | From Low Power Mode , ODR 1.6Khz |  | 1.5 |  | ms |
| BW | System Bandwidth |  |  | ODR/2 |  | Hz |
| OTR | Operating Temperature Range |  | -40 |  | 85 | ºC |
| STS | Temperature Sensor Slope |  |  | 1 |  | ºC/LSB |
| OTS | Temperature Sensor Offset |  |  | ±5 |  | ºC |

* 1. Absolute Maximum ratings

Stresses above absolute maximum ratings may cause permanent damage to device. Exceeding the specified

Characteristics may affect device reliability or cause mal-function.

Table 4. Absolute Maximum ratings

|  |  |  |  |
| --- | --- | --- | --- |
| **Symbol** | **Ratings** | **Maximum value** | **Units** |
| VDD | Supply voltage | -0.3 to 4.25 | V |
| VDDIO | I/O pin supply Voltage | -0.3 to 4.8 | V |
| OTR | Operating Temperature Range | -40 to 85 | ℃ |
| ESD | Electrostatic discharge protection(HBM) | 2 | KV |
| STG | Storage Temperature range | -50 to 150 | ℃ |
| MS | Mechanical Shock (<1ms) | 3000 | g |

1. Digital Interfaces

The SGA100 provides two different digital interfaces the I²C and SPI Serial interface.

The registers may be accessed through both the I²C and SPI serial interfaces for reading and writing.

The serial interfaces are mapped onto the same pads. To select I²C interface, CS line must be tied high

* 1. SPI Interface
     1. SPI Operation

The SPI Interface Uses 4-wires: SPC(Serial port Clock),SDI(serial data input),SDO(Serial data Output)

and CS(chip select).

CS is controlled by the SPI Master. Multiple read out is Possible.

SPI Transmission starts when CS goes to low and stops when CS goes to high: CS is Active low.

When CS is Active low, Data on SDI is latched by SGA100 at SPC Rising edge and SDO is changed at SPC

falling edge(SPI Mode3).



Figure 3. Four-Wire SPI Read and Write Protocol Diagram

Bit Definitions:

RW: SPI read and write mode significant bit flag. When RW is 0, the data(DI7-DI0) is written into the device.

When RW is 1, the data(DO7-DO0) is read from the device.

AD6-AD0: The address(7bit) of the device register.

DI7-DI0: The data(8bit) is written into the device.

DO7-DO0: The data(8bit) is read from the device.

* + 1. SPI Write



Figure 4. SPI Write Protocol

Bit Definitions:

RW: SPI write mode bit flag. The Value is 0

AD(6-0): The address of the device register.

DI(7-0): The data is written into the device.(MSB first)

The SPI Write command is performed with 16 clock pulses through SDI line as long as CS stays active low.

When write is required, two sequential bytes are necessary: one control byte to define the address to be written

and the one data byte.

Table 5. SPI Single Write Operation

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Start | Address1(0x11) | | | | | | | RW | Write Data(0xAA) | | | | | | | | Stop |
| CS=0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | CS=1 |



Figure 5. SPI Multiple write protocol Diagram

Bit Definitions:

RW: SPI Write mode bit flag. The Value is 0

AD(6-0): The address of the device register.

DI(7-0): The data is written into the device.(MSB first)

DI(15-8): Further data in multiple byte writing.(MSB first)

The SPI Multiple write mode also supported. After each byte of data is received, the register address is

internally incremented by one.

If a lot of data are transmitted and the highest address reached, the address will roll over to lowest address and the previously written data will be overwritten.

Table 6. SPI Multiple Write Operation

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Start | Address1(0x11) | | | | | | | RW | Address(0x12)-Write Data(0xAA) | | | | | | | | Address(0x13)-Write Data(0xAA) | | | | | | | | stop |
| CS=0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | CS=1 |

* + 1. SPI Read



Figure 6. SPI Single Read Protocol Diagram

Bit Definitions:

RW: SPI Read mode bit flag. The Value is 1

AD(6-0): The address of the device register.

DO (7-0): The data is read from the device. (MSB first)

The SPI Read command is performed with 16 clock pulses through SDI and SDO line as long as CS stays active low.

When Read access is required ,one control byte to define the address to be read followed by data byte.

Table 7. SPI Single Read Operation

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Start | Address1 (0x11) | | | | | | | RW | Read Data(0x1A) | | | | | | | | Stop |
| CS=0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | CS=1 |



Figure 7. SPI Multiple Read Protocol Diagram

Bit Definitions:

RW: SPI Read mode bit flag. The Value is 1

AD(6-0): The address of the device register.

DO(7-0): The data is read from the device.(MSB first)

DO(15-8): Further data in multiple byte reading.(MSB first)

Addresses are automatically incremented as long as CS stays active low**.** If the highest address reached,

the address will roll over to lowest address**.**

Table 8. SPI Multiple Read Operation

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Start | Address1 (0x11) | | | | | | | RW | Address1(0x11)-Read Data(0x1A) | | | | | | | | Address2(0x12)-Read Data(0x12) | | | | | | | | Address3(0x13)-Read Data(0x11) | | | | | | | | Stop |
| CS=0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | CS=1 |



Figure 8. Timing Diagram for SPI Interface

Table 9. SPI Timings

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Parameter | Symbols | Conditions | Min | Typical | Max | Unit |
| SPC Clock frequency | SCF |  |  |  | 10 | MHz |
| SPC Low Clock Time | SPC\_Low\_t |  | 20 |  |  | ns |
| SPC High Clock Time | SPC\_High\_t |  | 20 |  |  | ns |
| SDI Setup Time | SDI\_Setup\_t |  | 20 |  |  | ns |
| SDI Hold Time | SDI\_Hold\_t |  | 20 |  |  | ns |
| CS Setup Time | CS\_Setup\_t |  | 20 |  |  | ns |
| CS Hold Time | CS\_Hold\_t |  | 40 |  |  | ns |
| SDO Delay time | SDO\_Delay\_t |  |  |  | 30 | ns |

* 1. I²C Interface

The SGA100 I²C is a bus slave.

I²C Write Address of SGA100 is 11001000(0xC8), Read Address is 11001001(0xC9)

Only two bus lines are required; a serial data line (SDA) and a serial clock line (SPC).

These signals make it possible to support serial transmission of 8-bit bytes of data and 7-bit device addresses.

Both SDA and SPC are bidirectional lines, connected to VDDIO through external pull-up resistor.

When the bus is free, both the lines are high.

Data on the I2C-bus can be transferred at rates of up to 100kbit/s in the Standard-mode, up to 400kbit/s.

The I2C master is the CPU or microcontroller in the system.

Some microcontrollers even feature hardware to implement the I²C protocol.

You can also build an all-software implementation using a pair of general-purpose I/O pins.

* + 1. I²C Operation
* START and STOP Condition

START and STOP conditions are always generated by the master

All Transactions begin with START and are terminated by a STOP.

The Data Transfer on the bus Begins through a START signal.

Each data transfer must be terminated by the generation of a STOP condition.

A START condition is defined as a HIGH to LOW (falling edge) transition on SDA (SDI) while SPC is HIGH.

Stop Condition is LOW to HIGH (rising edge) transition on the SDA (SDI) while SPC is HIGH.

The START and repeated START conditions are functionally identical



Figure 9. I²C Start and Stop Timing diagram

* Data Transfer

One clock pulse(SPC) is generated for each data bit transferred.

The data on the SDA line must be stable during the HIGH period of the Serial port clock (SPC).

The HIGH or LOW state of the data line can only change when the clock signal on the SPC line is LOW.

Data is transferred with the Most Significant Bit (MSB) first.



Figure 10. I²C Bit Transfer Diagram

* Acknowledge& Not Acknowledge

The acknowledge takes place after every bytes.

The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received

And another byte may be sent.

The master generates all clock pulses, including the Acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA

Line LOW and it remains stable LOW during the HIGH period of this clock pulse. (Acknowledge signal)

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal



Figure 11. I²C Acknowledgement on SDA



Figure 12. Timing Diagram for I²C Interface

Table 10. I²C Timings

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Parameter | Symbols | Con | Min | Typical | Max | Unit |
| SPC Clock Frequency | ICF |  |  | 400 |  | KHz |
| Start Setup Time | Start\_Setup\_T |  | 160 |  |  | ns |
| Start Hold Time | Start\_Hold\_T |  | 160 |  |  | ns |
| Stop Setup Time | Stop\_Setup\_T |  | 160 |  |  | ns |
| SDA Setup Time | Data\_Setup\_T |  | 10 |  |  | ns |
| SDA Hold Time | Data\_Hold\_T |  | 10 |  | 70 | ns |
| SPC High Time | SPC\_Hight\_T |  | 60 |  |  | ns |
| SPC Low Time | SPC\_Low\_T |  | 160 |  |  | ns |
| New Data Transmit enable time | New\_Trans\_T |  | 100 |  |  | ns |

* + 1. I²C Write

After the START condition , a slave address is sent.

This address is seven bits long followed by an eighth bit which is a data direction bit (R/W):

a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ)

Master-transmitter transmits to slave-receiver. The transfer direction is not changed

The slave receiver acknowledges each byte.

A data transfer is always terminated by a STOP condition generated by the master.

Table 11. I²C Single Write Operation

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Conditions** | | | | | | | |
| **Master** | START | Slave Address+ W(0) |  | Register Address |  | Data |  | STOP |
| **Salve** |  |  | Ack |  | Ack |  | Ack |  |

After a start condition, a slave address(7bit) + W(zero) must be send.

If the slave acknowledge (ACK) has been returned, and then Data transfer is enabled.

The Master Transmitter is send to slave receiver one byte (register address): the 7 LSB represent

The actual register address and one dummy bit.

After Register address slave acknowledge (ACK), the Master is send to the slave receiver

one byte (register data).

It will be written to the register.

The I2C Multiple write mode also supported. After each byte of data is received, the register address is

internally incremented by one. If a lot of data are transmitted and the highest address reached, the address

will roll over to lowest address and the previously written data will be overwritten.

Table 12. I²C Multiple Write Operation

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Conditions** | | | | | | | | | |
| **Master** | START | Slave Address+W(0) |  | Register Address |  | Data |  | Data |  | STOP |
| **Salve** |  |  | Ack |  | Ack |  | Ack |  | Ack |  |

* + 1. I²C Read

A data transfer is always terminated by a STOP condition generated by the master.

However, if a master still wishes to communicate on the bus, it can generate a repeated START condition

and address another slave without first generating a STOP condition.

Table 13. I²C Single Read Operation

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Conditions** | | | | | | | |
| **Master** | START | Slave Address+W(0) |  | Register Address |  | Repeated Start | Slave Address+R(1) |  |
| **Salve** |  |  | Ack |  | Ack |  |  | Ack |

|  |  |  |
| --- | --- | --- |
| **Conditions** | | |
|  | No Ack | STOP |
| Data |  |  |

After a start condition, a slave address(7bit) + W(zero) must be send.

If the slave acknowledge (ACK) has been returned, and then Data transfer is enabled.

Master reads slave(SLAVE+R) immediately after first byte(Repeated START).

At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and

the slave-receiver becomes a slave-transmitter.

This first acknowledge is still generated by the slave.

The master generates subsequent acknowledges.

The STOP condition is generated by the master, which send a not-acknowledge just before the STOP condition.

Table 14. I²C Multiple Read Operation

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Device** | **Conditions** | | | | | | | |
| **Master** | START | Slave Address+W(0) |  | Register Address |  | Repeated Start | Slave Address+R(1) |  |
| **Salve** |  |  | Ack |  | Ack |  |  | Ack |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Conditions** | | | | | | |
|  | Master Ack |  | Master Ack |  | No Ack | STOP |
| Data |  | Data |  | Data |  |  |

After Repeated START and slave address+ R (one) acknowledge, address is automatically incremented.

If Master is Read data from SDA Line and Send Master Acknowledge to the slave, then slave automatically

send to next register address data On SDA Line.

1. Register Map
   1. List of the Registers

The table given below provides a listing of the 8 bit registers embedded in the device and the related address.

I²C Write Address of SGA100 is 11001000(0xC8), Read Address is 11001001(0xC9)

Table 15.Register Address Map

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Address** | **Name** | **Description** | **Type** | **Default** |
| 01h | DEV\_ID | Device ID | R | 0xA0 |
| 02h | STATUS | Device Status | R | - |
| 03h | CTRL\_REG1 | Control Register 1 | RW | 0x61 |
| 04h | CTRL\_REG2 | Control Register 2 | RW | 0xFC |
| 05h | CTRL\_REG3 | Control Register 3 | RW | 0x1A |
| 06h | OTP\_CTRL | OTP Control Register | RW | 0x04 |
| 07h | MANUAL\_BN\_SELECT CTRL | Manual Bank Control Register | RW | 0x00 |
| 08h | OTP TEST CTRL | OTP Test Control Register | RW | 0x00 |
| 09h | OTP TEST ADDRESS CTRL | OTP Test Address Register | RW | 0x00 |
| 0Ah | OTP TEST DATA CTRL | OTP Test Data Register | RW | 0x00 |
| 0Bh | OTP Bank Status | OTP Bank Usage Status Register | R | - |
| 0Ch | OTP PGM CYCLE | OTP Program Cycle Control Register | RW | 0xA0 |
| 0Dh~0Eh |  | T.B.D |  |  |
| 0Fh | TMODE\_CTRL | Test Mode Control Register | RW | 0x00 |
| 10h | INT1\_CTRL | Interrupt 1 Control | RW | 0x1A |
| 11h | INT1\_MAP\_FUNC | Interrupt1 Function Mapping | RW | 0x00 |
| 12h | OUT\_DATA\_XH | High Bytes of X- Axis Acceleration Data | R | - |
| 13h | OUT\_DATA\_XL | Low Bytes of X- Axis Acceleration Data | R | - |
| 14h | OUT\_DATA\_YH | High Bytes of Y- Axis Acceleration Data | R | - |
| 15h | OUT\_DATA\_YL | Low Bytes of Y- Axis Acceleration Data | R | - |
| 16h | OUT\_DATA\_ZH | High Bytes of Z- Axis Acceleration Data | R | - |
| 17h | OUT\_DATA\_ZL | Low Bytes of Z- Axis Acceleration Data | R | - |
| 18h | OUT\_DATA\_TEMP | 8bit Temperature Data | R | - |
| 19h | USR\_GAIN \_X\_CTRL | User set gain on X-axis(x0-x2). | RW | 0x80 |
| 1Ah | USR\_GAIN \_Y\_CTRL | User set gain on Y-axis(x0-x2). | RW | 0x80 |
| 1Bh | USR\_GAIN \_Z\_CTRL | User set gain on Z-axis(x0-x2). | RW | 0x80 |
| 1Ch | USR \_OFS\_X\_CTRL | User set offset on X-axis.(x64) | RW | 0x00 |
| 1Dh | USR \_OFS\_Y\_CTRL | User set offset on Y-axis.( x64) | RW | 0x00 |
| 1Eh | USR \_OFS\_Z\_CTRL | User set offset on Z-axis. (x64) | RW | 0x00 |
| 1Fh | TEST\_CTRL | OFFSET Enable Control (Reserved) | RW | 0x00 |
| 20h~32h |  | T.B.D |  |  |
| 33h | DIGITAL\_FILTER\_CTRL | Digital filter control | RW | 0x00 |
| 34h | INT\_FUNC\_CTRL1 | FIFO/NDR Interrupt Control | RW | 0x00 |
| 35h | INT\_FUNC\_CTRL2 | Motion Interrupt Control | RW | 0x80 |
| 36h | INT\_FUNC\_CTRL3 | Tap/Double Tap Interrupt Control | RW | 0x00 |
| 37h | FIFO\_CTRL | FIFO Control | RW | 0x00 |
| 38h | FIFO\_DATA\_STATUS | FIFO Stored level status | R | - |
| 39h | INT\_FUNC\_CTRL1\_STATUS | FIFO /NDR Interrupt Status | R | - |
| 3Ah | MOTION\_CTRL | Motion Detection Mode Control | RW | 0x00 |
| 3Bh | MOTION\_STATUS | Motion Interrupt status | R | - |
| 3Ch | MOTION\_HIGH\_TH | High Event Threshold | RW | 0xBE |
| 3Dh | MOTION\_HIGH\_DUR | High Event Duration | RW | 0x02 |
| 3Eh | MOTION\_LOW\_TH | Low Event Threshold | RW | 0x2D |
| 3Fh | MOTION\_LOW\_DUR | Low Event Duration | RW | 0x02 |
| 40h | TAP\_INT\_STATUS | Tap /Dtap Interrupt status | R | - |
| 41h | TAP\_TH | Tap Detection Threshold | RW | 0x40 |
| 42h | TAP\_DUR | Tap Detection Time Limit | RW | 0x07 |
| 43h | DTAP\_TIMEWINDOW\_DUR | Double Tap Detection Window Duration | RW | 0x28 |
| 44h | TAP\_LATENCY\_DUR | Tap Detection Latency | RW | 0x05 |
| 45h~4Bh |  | T.B.D |  |  |
| 4Ch | AFE\_WT\_MODE | AFE Wafer Level Test Mode Selection | RW | 0x00 |
| 4Dh | CMI | Main Bias Current Control | RW | 0x04 |
| 4Eh | TEST\_DREGISTER | Digital Register file Test Control | RW | 0x0 |
| 4Fh | TEST\_DREGISTER\_STATUS | Digital Register Test Status | R |  |
| 50h | CP\_ OT\_PX | X channel positive capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 51h | CP\_ OT\_NX | X channel negative capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 52h | CP\_ OT\_PY | Y channel positive capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 53h | CP\_ OT\_NY | Y channel negative capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 54h | CP\_ OT\_PZ | Z channel positive capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 55h | CP\_ OT\_NZ | Z channel negative capacitor offset trimming level(0~310fF) | RW | 0x00 |
| 56h | PGA \_GT\_XY | X/Y channel PGA Gain Trimming (2~4.5) | RW | 0x66 |
| 57h | PGA \_GT\_Z | Z channel PGA Gain Trimming(2~4.5) And PGA Mode Select | RW | 0x60 |
| 58h | TOSC3\_VBGR | OSC1 Temp. Compensation, Band Gap Reference Trimming | RW | 0x78 |
| 59h | DVP | 0.9V Reference Trimming | RW | 0x10 |
| 5Ah | TSEN\_DC | Temperature Offset trimming | RW | 0x02 |
| 5Bh | TOSC1 | 1.6Mhz OSC Clock trimming | RW | 0x3F |
| 5Ch | TOSC2 | 25khz OSC Clock trimming | RW | 0x1F |
| 5Dh | DFACT\_GT\_X | Digital Factory Gain Fine- trimming for X- Axis(x0~x4) | RW | 0x40 |
| 5Eh | DFACT\_GT\_Y | Digital Factory Gain Fine- trimming for Y- Axis(x0~x4) | RW | 0x40 |
| 5Fh | DFACT\_GT\_Z | Digital Factory Gain Fine- trimming for Z- Axis(x0~x4) | RW | 0x40 |
| 60h | DFACT\_OFS\_XYZ | Digital Factory Offset trimming direction control | RW | 0x07 |
| 61h | DFACT\_OT\_X | Digital Factory Offset Fine- trimming for X- Axis(scale: x64) | RW | 0x00 |
| 62h | DFACT\_OT\_Y | Digital Factory Offset Fine- trimming for Y- Axis(scale: x64) | RW | 0x00 |
| 63h | DFACT\_OT\_Z | Digital Factory Offset Fine- trimming for Z- Axis(scale: x64) | RW | 0x00 |
| 64h | DSIGN\_CONTROL | Digital Axis Signal Control | RW | 0x00 |
| 65h | OTP\_PM | OTP Power Mode Control | RW | 0x01 |
| 66h~6Fh |  | T.B.D |  |  |
| 70h | OFFSET\_DATA\_MSB | Offset Data MSB Status | R |  |
| 71h | OFFSET\_DATA\_LSB | Offset Data LSB Status | R |  |

Registers marked as ***Reserved*** must not be changed. The Writing to those Register may cause Operation Fail and Damage to the device

|  |  |
| --- | --- |
| color | Access description |
|  | OTP Register(HIDDEN) |
|  | T.B.D(HIDDEN) |
|  | RESERVED(HIDDEN) |
|  | Normal Register |

1. RegisterDescription
   1. DEV\_ID (01h)

SGA100의 모델/REVISION등을 구분할 수 있는 Identifier

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| ID[7:0] | | | | | | | |

DEV\_ID Register(R/O)

Initial value: 0xA0 (SGA100)

|  |  |
| --- | --- |
| **Name** | **Description** |
| ID [7:0] | Device identifier Of SGA100 |

* 1. STATUS Register (02h)

센서의 Sleep to Wakeup상태 및 New Data Available의 상태/Initialized상태정보를 표시.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  | | 5 | 4 | 3 | 2 | 1 | 0 |
|  | Reserved |  | SWRD | NDR\_Z | NDR\_Y | NDR\_X | WKUPD | INITD |

STATUS Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| SWRD | Status of Soft Reset  0:None  1:Soft Reset Done(Soft Reset동작 완료시 1로 설정 )->읽어가면0으로. |
| NDR\_Z | New data Ready for Z axis  .  0: Not Ready  1: New data available for Z Axis |
| NDR\_Y | New data Ready for Y axis  0: Not Ready  1: New data available for Y Axis |
| NDR\_X | New data Ready for X axis  0: Not Ready  1: New data available for X Axis |
| WKUPD | Status of Sleep to Wakeup  0: No Wake Up (Sleep to wake up을 disable하거나 Power mode가 Low Power mode 이외로 바뀌었을 경우 0 Clear)  1:Sleep to Wakeup done (Sleep to wake up 동작 발생시 1) |
| INITD | Status of Initialization(Reload,Power On/POR/SWR)  0: No Init  1: Auto Init done ->초기 전원이 인가되어 ROM과 각종 블록의 설정이 자동으로 로딩이 완료되면 1로 설정된다. |

NDR X/Y/Z Status는 각축의 New Data가 Output Register에 Update되면 1로 설정되고 각 축의 LSB/MSB를 읽어가면 0 Clear된다.읽어가지 않는다면 계속 업데이트 되므로 1이 된다. (Update정책은 Block Data Update와 연계된다.)

* 사용자가 다음 Data를 읽기 전에 상태가 0이면 새로운 Data가 Update되기 전에 빠른 상태로 다시 읽는 것이고 1인 상태라면 Update된 후에 읽는 상태이다
  1. CTRL\_REG1 Register (03h)

Power/Sleep duration/ODR설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 |  | 3 | 2 |  | 0 |
| Power\_Down | PM | Sleep\_Dur | | | ODR | | |

CTRL\_REG1 Register(R/W)

Initial value: 0x61

|  |  |
| --- | --- |
| **Name** | **Description** |
| ODR[2:0] | Output Data Rate Selection In Normal Mode. Default:001  000: ODR =25 Hz  001: ODR =50 Hz(default)  010: ODR =100 Hz  011: ODR =200 Hz  100: ODR =400 Hz  101: ODR =780 Hz  110: ODR =1600hz  111: ODR =3000hz-Bypass LPF |
| Sleep\_Dur[5:3] | Low Power Mode일 때 Sleep 시간 설정. Default: 100  Normal Mode로 전환되고 한개의Sample이 나오는 소요시간은 ODR에 따른 Sampling이 다 끝나야 하므로 빠른 ODR일때는 짧고 느린 ODR일때는 길다.  000: Sleep Duration 2s  001: Sleep Duration 1s  010: Sleep Duration 500ms  011: Sleep Duration 100ms  100: Sleep Duration 50ms(default)  101: Sleep Duration 25ms  110:Not Used  111:Not Used |
| PM | Configuration of Main power modes. Default value: 1.  0: Low Power Mode  1: Normal Mode |
| Power\_Down | Controls device power down. Default value: 0  0: Disable  1: Enable |

* 1. CTRL\_REG2 Register (04h)

3축의 Sensing Control/Full Scale/User Offset Sign Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ZEN | YEN | XEN | ZOS | YOS | XOS | FS | |

CTRL\_REG2 Register(R/W)

Initial value: 0xFC

|  |  |
| --- | --- |
| **Name** | **Description** |
| ZEN | Z-Axis Enable. Default: 1  1: Enabled. (default).  0: Disabled |
| YEN | Y-Axis Enable. Default: 1  1: Enabled. (default).  0: Disabled |
| XEN | X-Axis Enable. Default: 1  1: Enabled. (default).  0: Disabled |
| ZOS | User Z Offset의Positive/Negative 적용을 선택(User Offset은 Default가 0이므로 어느 방향으로 기본값이 되던 상관없음) Default: 1  1: Positive Direction (default).  0: Negative Direction |
| YOS | User Y Offset의Positive/Negative 적용을 선택 Default: 1  1: Positive Direction (default).  0: Negative Direction |
| XOS | User X Offset의Positive/Negative 적용을 선택 Default: 1  1: Positive Direction (default).  0: Negative Direction |
| FS | Full Scale Selection Default: 0  00- 2g (default).  01- 4g  10- 8g  11- 16g |

* 1. CTRL\_REG3 Register (05h)

소프트리셋/Self Wake Up/Data sync/

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | WatchDis | PDRstEn | SWRstMD | SOFT\_RST | BDU | SWM |

CTRL\_REG3 Register(R/W)

Initial value: 0x1A

|  |  |
| --- | --- |
| **Name** | **Description** |
| WatchDis | Reserved  0: default |
| PDRstEn | Reserved, Power Down시 내부 Logic 초기화 Default: 1  0 : Disable  1 : Enable (default) |
| SWRstMD | Reserved, SOFT\_RST 시 Register도 Reset Default: 1  0 : SOFT\_RST 시 내부 Logic만 초기화 되고 Register는 변하지 않음  1 : SOFT\_RST 시 내부 Logic 및 Register 모두 초기화 (default) |
| SOFT\_RST | 모든 설정사항을 내부 ROM으로 부터 읽어 들여 초기화(HW Reset=POR과 같은 역할) Default: 0  1: Reset->완료되면 Status Register의 SWRD bit에 업데이트되어야 한다. Reset완료후 다시 0으로 Clear  0: No Reset(default) |
| BDU | Output data register 읽기 시 무결성을 위해 Data Update를 읽는동안 Block시킬 것인지 설정. Default: 1  0: Not Blocked.  1: Blocked Output Data Register between MSB and LSB reading(default) |
| SWM | Sleep to Wake up Mode Default: 0  Low power mode로 동작 중 Interrupts발생시 Normal mode로 복귀할 것인가 설정..  1: Enabled  0: Disabled(default) |

Sleep to Wakeup 으로Interrupt가 발생해 Normal로 ODR로 전환되었을 때 다시 Low Power Mode로 돌아가는 조건은 Sleep to wakeup을 disable 시켜주는 방법 뿐이다. (Low Power 내의 다른 낮은 hz(Sleep Duration)의 옵션을 선택했을 때는 계속 Normal ODR로 동작)

Sleep to Wake Up으로 깨어난 동작 상태(Low Power상태)에서

Low Power 이외의 다른 Power Mode(Normal과 PowerDown) 를 선택함으로써 Low Power Mode에서 해당 Power Mode로 전환됨.(Wakeup Done Clear, Sleep to Wakeup설정은 그대로 남아있음)

Soft Reset시 Reset이 안되는 Block은 I2C/SPI Block.

* 1. OTP\_CTRL Register (06h)

OTP동작 Control Register.

- ReLoad\_OTP 실행 시 Manual로 지정된 Bank내의 0h부터~최대64h까지의 OTP에 저장된 Calibration정보를 0x50h~0x64h의 Calibration Control Register에 자동으로 적용된다.

- WEN\_OTP실행 시 Calibration Register 0x50h~0x64h전체가 자동으로 새로운 최신뱅크를 선택해 0h~최대64h에 자동으로 OTP에 Write된다. (이때 Bank0의 Bank Usage플래그도 자동으로 설정되어야 한다)

0~7번 Bank(8개)

0번 Bank는 Bank Usage Flag(0xff: 사용되지 않음 0xA0:사용됨)-직접적으로 쓰지 않는 것이 좋다..

1번~ 7번 Bank를 실제 사용.(0번 Bank를 Manual OTP Test 로 사용할 때 잘못 쓰면 정상 동작안됨)

부팅 시 가장 마지막에 쓰여진 Bank의 정보를 자동 Load해서 적용됨.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | reserved | CLKSEL | reserved | WPT\_OTP | ReLoad\_OTP | WEN\_OTP |

OTP\_CTRL Register(R/W)

Initial value: 0x04

|  |  |
| --- | --- |
| **Name** | **Description** |
| CLKSEL  (Reserved) | PKG이후 OTP Programming시 내부 Clock이 OTP Programming Timing을 만족시키지 못할 경우 이 bit를 Enable시키고 INT Pin에 clock을 입력시켜 Programming시킬 수 있다.  CLKSEL을 1로 setting 시 INT Pin에 1.6MHz CLOCK을 입력시키면 내부에서는 Analog에서 만들어진 1.6MHz를 사용하지 않고 INT Pin으로 입력된 Clock을 사용하게 된다. 이때 내부 Logic은 정상적으로 동작되지 않지만 OTP Programming은 정상적으로 동작 된다. Default: 0  0: 내부 Analog 1.6Mhz Clock사용하여 OTP programming진행(default)  1: INT1 Pin을 통한 외부 1.6Mhz Clock사용하여 Programming진행. |
| WPT\_OTP | Write Protection (Write Operation이 되지 않게 함) //OTP Manual Test모드에도 적용.. Default: 1  1: Enable (default) //Write Protection  0: Disable |
| ReLoad\_OTP | (Manual Bank Register에 지정한 Bank의 정보전체를 Register에 로드하고 적용함.) Default: 0  0:Disable(default)  1:ReloadRoad가 끝난 후 다시 0으로 Clear |
| WEN\_OTP | OTP에 전체 Calibration Register data의 Write Operation를 수행. Default: 0  0: No Write(default)- 쓰기가 완료되면 자동으로 0으로 클리어.  1: Write(Update All OTP Register Data to OTP Memory)-자동으로 현재 쓴 가장 마지막 뱅크의 다음뱅크가 쓰여짐)  0번 뱅크의 Bank사용Flag를 동시에 자동으로 0xA0로 설정  쓰고 난 후 일정시간(us)대기 실제로 써질 시간 동안 대기해야 함. |

* 1. MANUAL\_BN\_SELECT CTRL Register (07h)

Reload및 수동으로 Write/Read 할 Tareget Bank의 Number를 지정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 |  |  | 0 |
| reserved | reserved | reserved | reserved | Manual\_BN | | | |

Manual\_Bn\_Select CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| Manual\_BN [3:0] | Bank Number(0~7)//Taget Bank. |

* 1. OTP TEST CTRL Register (08h)

Manual 로 OTP 특정 뱅크의 Address의 Data를 Read/Write를 Control.

Manual로 OTP bank를 Control시 절차에 맞는 사용을 하지 않을 경우 사용할 수 없는 문제가 발생(한 개의 뱅크를 모두 사용한 후 반드시 0번 Bank에 사용한 Bank에 해당하는 Flag를 설정해야 한다.)

Manual로 사용할 경우 사용자 부주의가 생기지 않도록 조심 해야 한다.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | | | 1 | 0 | |
| APG | MR | reserved | reserved | reserved | | Reserved | MODE\_SELECT | | | Instruction |

OTP test CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| APG (Reserved) | OTP TEST CONTROL |
| MR(Reserved) | OTP TEST CONTROL |
| MODE\_SELECT | Manual bank access Mode selection. Default: 0  0: Read Mode(default)  1: Write Mode |
| Instruction | Command. Default: 1  1: Instruction Execute //Execute를 실행해서 쓰기가 완료되면 다시 0으로 돌아온다. //Write동작은 Write Protection이 1이면 수행되지 않는다.  0: No Execute(default) |

* 1. OTP TEST ADDRESS Register (09h)

Manual OTP Test Control Address지정.

-Manual로 OTP Bank내의 특정Address정보를 Read와 Write시 Target Bank의 (0h~최대63h)의 Address가 설정되어야 함.

- Manual 로 OTP bank내의 0h~63h의 Address에 Data를 쓰는 것은 50h~65h의 Calibration Control Register에 영향을 주지 않는다. 실제 50h~65h에 적용될려면 Reload를 하거나 리부팅(가장 마지막 최신뱅크내용으로 자동으로 로딩)을 거치면 된다.

-Manual로 OTP에 특정 Bank의 0h~63h의 정보를 읽으면 이 값은 OTP Test Data Register에만 읽은 값이 저장되어 모니터링 될뿐 50h~65h의 Calibration control Register에 적용되지 않는다.

-OTP Test Address는 0~63h로 Bank Address로 Bank Address 0h는 OTP Register인 50h register정보와 일치하고 나머지도 차례대로 일치한다.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 |  |  | 0 |
| Address | | | | | | | |

OTP test address Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| Address[7:0] | 8 bit OTP Address(0-63번지)//각 Bank내의 0~63번지 |

* 1. OTP TEST DATA Register (0Ah)

-Manual로 특정Bank내의 특정 Address에 쓰거나 읽을 Data (50h~65h의 실제Calibration Control Register에 적용되지 않음)

-Manual Write시 특정 OTP Bank의 0h~63h에 Write할 data지정

-Manual Read시 특정 OTP Bank의 0h~63h의 읽어온 정보가 저장됨..

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 |  |  | 0 |
| Data | | | | | | | |

OTP test data register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| Data[7:0] | 8 bit Data |

* 1. OTP BANK STATUS Register (0Bh)

현재 Bank의 사용 내역을 Flag로 표시. (0xff:뱅크가 사용되지 않음-> 0으로 Status 표기 0xA0:뱅크가 사용됨은-> 1로 Status표기)

뱅크 0의 0번지는 사용하지 않고, Bank0의 1번지~7번지까지 1~7번 뱅크 사용 정보표시.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 |
| BNK7 | BNK6 | | BNK5 | | BNK4 | | BNK3 | | BNK2 | | BNK1 | | Reserved | |

OTP Bank Status Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| BNK7 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음.(default) |
| BNK6 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |
| BNK5 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |
| BNK4 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |
| BNK3 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |
| BNK2 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |
| BNK1 | 1: 해당 Bank 사용됨  0: 해당 Bank가 아직 사용되지 않음. (default) |

* 1. OTP PGM Cycle Register (0Ch)

OTP의 Write시의 typical time: 1.6Mhz로 160 clock count시간 동안 Write(100us)

만약 OSC1이 1.6Mhz보다 빨라지면 위의 Typical Time(100us)이 되도록 clock count를 조절해야 함

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTP\_PGM [7:0] | | | | | | | |

OTP PGM Cycle Register(R/W)

Initial value: 0xA0

|  |  |
| --- | --- |
| **Name** | **Description** |
| OTP\_PGM [7:0] | 0xA0(default) |

INT1\_PRD\_TIME CTRL Register (기능 지원 안됨, Register 삭제)

Interrupt 1이 인터럽트 발생 후 일정 시간 후에 Clear(interrupt1의 Mode가 Periodic일 경우 적용.)//

INT\_RST이 수행되면 바로 Clear된다.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ~~INT1\_PRD~~ | | | | | | | |

INT1\_PRD\_TIME CTRL Register(R/W)

INT1\_PRD

25HZ~400HZ까지는 1/ODR의 시간에 의존하여 (INT1\_PRD+1) 가 내부적으로 측정에 사용되고 나머지ODR(700~ODRMax)는 4/ODR의 시간에 의존하여 내부적으로 사용된다.

Low Power Mode일 때는 Sleep+wakeup+샘플링 시간에 의존하여 (INT1\_PRD+1) 가 사용된다.

|  |  |  |  |
| --- | --- | --- | --- |
| INT1\_PRD | **ODR** | **Normal Mode** | **Low Power Mode** |
| (0~255) | ≤400HZ | (INT1\_PRD+1) \* (1/ODR) sec | (INT1\_PRD+1)\*( Sleep+Wakeup+Sampling Time ) |
| >400Hz | (INT1\_PRD+1) \* (4/ODR) sec |

Initial value: 0x0

|  |  |
| --- | --- |
| **Name** | **Description** |
| ~~INT1\_PRD[7:0]~~ | 0// 0이면 Interrupt Clear Time이 0이 되므로 내부적으로 INT1\_PRD +1을 해서 사용한다. |

* 1. TMODE\_CTRL Register (0Fh)

CLK\_SEL가 0 일 때 Int1 pin을 통한 Testmode시의 signal output 동작설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEST\_DEN | reserved | reserved | reserved | TEST\_D | | | |

TMODE\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| TEST\_DEN | INT PIN이 Test Signal Out 용도로 동작하게 설정. Default: 0  0: Normal INT Pin Operation.  1: TEST\_D[3:0]에 설정된 signal이 INT Pin1을 통해 출력. |
| TEST\_D[3:0] | Analog I/F Test Signal Selection. Default: 0  0000: SLEEP\_ENB (to analog)  0001: XC( to Analog)  0010: YC( to Analog)  0011: ZC( to Analog)  0100: TC( to Analog)  0101: (XC or YC or ZC or TC)  0110: OTP\_PM( 25KHz Clock Delayed Signal) ( to Analog)  0111: OTP\_PM Register( to Analog)  1000: I\_AD\_VAL( from Analog)  1001: I\_X ( from Analog)  1010: I\_Y ( from Analog)  1011: I\_Z ( from Analog)  1100: (I\_X or I\_Y or I\_Z or I\_T) ( from Analog)  1101: I\_AD\_DAT (from Analog)  1110: 25KHz Clock ( from Analog)  1111: 1.6MHz Clock ( from Analog) |

* 1. INT1\_CTRL Register (10h)

Not Latched - Interrupt 조건을 만족하는 상황이 유지된다면 계속 Interrupt가 유지

Latched - INT1\_RST을 통해 Clear하기 전까진 계속 유지.

INT1\_RST은 Not latched Mode나 Latched Mode구분 없이 Latch상태를 클리어 함.

-New Data Ready Interrupt는 새로운 X,Y,Z Data를 획득 완료하여 Update시 발생

Not Latched Mode일 때 (Enable)활성화된 축의 Output Data Register가 모두 읽어지면 New Data Ready Interrupt Clear발생/Output Register 를 읽어가지 않는다면 그대로 Interrupt유지

Latched Mode일 때는 INT1\_RST을 통해 Clear하기 전까진 계속 유지(New Data Ready Interrupt는 Not Latched Mode를 권장)

-Tap/DTap은 인터럽트 발생 후 입력무시 시간 동안(그것도Tap상황이므로) interrupt를 유지하다가 입력 무시가 끝나는 순간clear한다.

Interrupt1 pin의 동작설정을Control..

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 0 |
| reserved | reserved | reserved | INT1\_ACTIVE\_LEVEL | INT1\_PP\_SELECT | Reserved | | INT1\_MODE | INT1\_RST |

INT1\_CTRL Register(R/W)

Initial value: 0x1A

|  |  |
| --- | --- |
| **Name** | **Description** |
| INT1\_ACTIVE\_LEVEL | 1: Active High (default).  0: Active Low |
| INT1\_PP\_SELECT | Push- Pull / Open drain.  1: Push-Pull (default)  0: Open drain. |
| INT1\_MODE | Interrupt1 Mode Selection (1bit으로 변경)  1: NOT Latch Interrupt (default).  0: Latch Interrupt |
| INT1\_RST | Interrupt 1 Reset(Clear Latch)  1:Reset //Clear 후에 다시 0로  0:NONE(default) |

* 1. INT1\_MAP\_FUNC Register (11h)

Interrupt Function의 동작을 Interrupt Pin1에 Mapping

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | reserved | reserved | MAP\_FIFO | MAP\_MOTION | MAP\_TAP\_DTAP | MAP\_DRDY |

INT1\_MAP\_FUNC Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| MAP\_FIFO | map FIFO interrupt to INT1 Pin(Fifo Full/Watermark/Empty)  1:Enable  0:Disable(Default) |
| MAP\_MOTION | map Motion Interrupt to INT1 Pin(Z/Y/X Low High Event)  1:enable  0:Disable(Default) |
| MAP\_TAP\_DTAP | map Tap/Double Tap Interrupt to INT1 Pin  1:enable  0:Disable(Default) |
| MAP\_DRDY | Map New Data Ready Interrupt o INT1 Pin  1: enable  0: Disable(Default) |

* 1. OUT\_DATA\_XH Register (12h)

X-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| XH[15:8] | | | | | | | |

OUT\_DATA\_XH Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| XH[15:8] | X- Axis acceleration data.  The value is expressed in two’s complement with 8bit High Byte |

* 1. OUT\_DATA\_XL Register (13h)

X-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| XL[7:0] | | | | | | | |

OUT\_DATA\_XL Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| XL[7:0] | X- Axis acceleration data.  The value is expressed in two’s complement with 8bit Low Byte |

* 1. OUT\_DATA\_YH Register (14h)

Y-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| YH[15:8] | | | | | | | |

OUT\_DATA\_YH Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| YH[15:8] | Y- Axis acceleration data.  The value is expressed in two’s complement with 8bit High Byte |

* 1. OUT\_DATA\_YL Register (15h)

Y-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| AY\_D[7:0] | | | | | | | |

OUT\_DATA\_YL Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| YL[7:0] | Y- Axis acceleration data.  The value is expressed in two’s complement with 8bit Low Byte |

* 1. OUT\_DATA\_ZH Register (16h)

Z-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| ZH[15:8] | | | | | | | |

OUT\_DATA\_ZH Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| ZH[15:8] | Z- Axis acceleration data.  The value is expressed in two’s complement with 8bit High Byte |

* 1. OUT\_DATA\_ZL Register (17h)

Z-axis Acceleration data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| ZL[7:0] | | | | | | | |

OUT\_DATA\_ZL Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| ZL[7:0] | Z- Axis acceleration data.  The value is expressed in two’s complement with 8bit Low Byte |

* 1. OUT\_DATA\_TEMP Register (18h)

1도/1LSB의 Slope

Temperature data is stored this register. This register is a read only.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| TEMP[7:0] | | | | | | | |

OUT\_DATA\_TEMP Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| TEMP[7:0] | 8bit Temperature data.  The value is expressed in two’s complement  0x0:23ºC 를 나타냄. |

* 1. USR\_GAIN\_X\_CTRL Register (19h)

사용자가 Sensitivity를x 0~x2(x1.99)배까지 추가적으로 Gain Control하기 위함. (ROM에 저장된Factory trimming된 Total gain 에 추가로 적용됨.)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| GAIN\_X[7:0] | | | | | | | |

USR\_GAIN\_X\_CTRL Register(R/W)

Initial value: 0x80

|  |  |
| --- | --- |
| **Name** | **Description** |
| GAIN\_X[7:0] | Gain values for Sensitivity trimming of X-axis.  The value is expressed in unsigned format.  Total gain range:x0~x2  Default Value:0x80(x1) |

* 1. USR\_GAIN\_Y\_CTRL Register (1Ah)

사용자가 Sensitivity를x 0~x2(x1.99)배까지 추가적으로 Gain Control하기 위함. (ROM에 저장된Factory trimming된 Total gain 에 추가로 적용됨.)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| GAIN\_Y[7:0] | | | | | | | |

USR\_GAIN\_Y\_CTRL Register(R/W)

Initial value: 0x80

|  |  |
| --- | --- |
| **Name** | **Description** |
| GAIN\_Y[7:0] | Gain values for Sensitivity trimming of Y-axis.  The value is expressed in unsigned format.  Total gain range:x0~x2  Default Value:0x80(x1) |

* 1. USR\_GAIN\_Z\_CTRL Register (1Bh)

사용자가 Sensitivity를x 0~x2(x1.99)배까지 추가적으로 Gain Control하기 위함. (ROM에 저장된Factory trimming된 Total gain 에 추가로 적용됨.)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| GAIN\_Z[7:0] | | | | | | | |

USER\_GAIN\_CTRL\_Z Register(R/W)

Initial value: 0x80

|  |  |
| --- | --- |
| **Name** | **Description** |
| GAIN\_Z[7:0] | Gain values for Sensitivity trimming of Z-axis.  The value is expressed in unsigned format.  Total gain range:x0~x2  Default Value:0x80(x1) |

* 1. USR\_OFS\_X\_CTRL Register (1Ch)

User가 Offset을 추가로Calibration하기 위해 설정.(ROM에 저장된Factory trimming된 Offset 에 추가로 적용됨.)

**± 0~16384COUNT** 의 Offset을 Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| OFS\_X[7:0] | | | | | | | |

USR\_OFS\_X\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFS\_X[7:0] | Offset values for Offset trimming of X-axis.  The value is expressed in unsigned format.  CTRL\_Reg2의 XOS bit에 따라 Positive/negative방향으로 적용  Scale Factor:x64  default : 0 |

* 1. USR\_OFS\_Y\_CTRL Register (1Dh)

User가 Offset을 추가로Calibration하기 위해 설정.(ROM에 저장된Factory trimming된 Offset 에 추가로 적용됨.)

**± 0~16384COUNT** 의 Offset을 Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| OFS\_Y[7:0] | | | | | | | |

USR\_OFS\_Y\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFS\_Y[7:0] | Offset values for Offset trimming of Y-axis.  The value is expressed in unsigned format.  CTRL\_Reg2의 YOS bit에 따라 Positive/negative방향으로 적용  Scale Factor:x64  default : 0 |

* 1. USR\_OFS\_Z\_CTRL Register (1Eh)

User가 Offset을 추가로Calibration하기 위해 설정.(ROM에 저장된Factory trimming된 Offset 에 추가로 적용됨.)

**± 0~16384COUNT** 의 Offset을 Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| OFS\_Z[7:0] | | | | | | | |

USR\_OFS\_Z\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFS\_Z[7:0] | Offset values for Offset trimming of Z-axis.  The value is expressed in unsigned format.  CTRL\_Reg2의 ZOS bit에 따라 Positive/negative방향으로 적용  Scale Factor:x64  default : 0 |

* 1. TEST\_CTRL Register (1Fh)

OFFSET Enable Control (Reserved) : 0x70, 0x71 Offset Data //Enable시 0x70,0x71에 X,Y,Z출력은 멈추고Offset값이 출력된다.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | reserved | reserved | reserved | reserved | reserved | OFF\_EN |

TEST\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFF\_EN | Enable/Disable Offset Value Display default: 0  1: Enable  0: Disable |

* 1. DIGITAL\_FILTER\_CTRL Register (33h)

Digital Filter의 선택 설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | reserved | reserved | INT\_SRC | OUTPUT\_SRC | HPF\_FREQ | |

DIGITAL \_FILTER\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| INT\_SRC | Interrupt Data Source 선택  0: Low Pass Filter Data(Default)  1: High Pass Filter Data |
| OUTPUT\_SRC | Output Data Source 선택  0: Low Pass Filter Data(Default)  1: High Pass Filter Data |
| HPF\_FREQ[1:0] | High Pass Filter Loll off frequency  ODR 3Khz일 때  00: 64hz(default)  01: 32hz  10: 16hz  11: 8hz |

* 1. INT\_FUNC\_CTRL1 Register (34h)

Fifo Interrupt와 NDR Interrupt를 Enable/Disable Control.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| reserved | reserved | reserved | reserved | FWTM\_EI | FFULL\_ EI | FEMPTY\_ EI | NDR\_ EI |

INT\_FUNC\_CTRL1 Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| FWTM\_EI | Enable interrupt for FIFO watermark  0: Disabled (default).  1: Enabled. |
| FFULL\_EI | Enable interrupt for FIFO full  0: Disabled (default).  1: Enabled |
| FEMPTY\_EI | Enable interrupt for FIFO Empty  0: Disabled (default).  1: Enabled |
| NDR\_EI | Enable interrupt for New Data Ready  0: Disabled (default).  1: Enabled |

-Not latched Mode일 때

Buffer Full interrupt는 Buffer를 읽어가면 clear된다.

Watermark는 Watermark count 수를 초과하면 발생하고 아래로 떨어지면 Clear된다.

* 1. INT\_FUNC\_CTRL2 Register (34h)

Motion Interrupt Enable/Disable Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AO\_MI | ZHIE | YHIE | XHIE | DIR\_EN | ZLIE | YLIE | XLIE |

INT\_FUNC\_CTRL2 Register(R/W)

Initial value: 0x80

|  |  |
| --- | --- |
| **Name** | **Description** |
| AO\_MI | AND/OR combination of Motion Interrupt events.  0 : AND combination of interrupt events  1 : OR combination of interrupt events(default). |
| ZHIE | Enable interrupt generation on Z high event.  0 : Disable interrupt (default).  1 : Enable interrupt |
| YHIE | Enable interrupt generation on Y high event.  0 : Disable interrupt (default).  1 : Enable interrupt |
| DIR\_EN | Enable Direction Mode  0: No Direction Mode- Absolute Output Value(Default)  1: Enable Direction Detection |
| XHIE | Enable interrupt generation on X high event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| ZLIE | Enable interrupt generation on Z low event.  0 : Disable interrupt (default).  1 : Enable interrupt |
| YLIE | Enable interrupt generation on Y low event.  0 : Disable interrupt (default).  1 : Enable interrupt |
| XLIE | Enable interrupt generation on X low event.  0 : Disable interrupt (default).  1 : Enable interrupt |

* 1. INT\_FUNC\_CTRL3 Register (35h)

Single Tap/Double Tap interrupt Enable/Disable Control

Single과 double이 동시에 Interrupt가 설정됐을 경우 double Tap 입력을 했다면 SingleTap detection Interrupt가 발생 후 Double tap Interrupt발생.(Bosch의 그림참조)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AO\_DTI | ZDTIE | YDTIE | XDTIE | AO\_STI | ZSTIE | YSTIE | XSTIE |

INT\_FUNC\_CTRL3 Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| AO\_DTI | And/or combination of Double Tap Interrupt events.  0 : AND combination of interrupt events (default).  1 : OR combination of interrupt events |
| ZDTIE | Enable interrupt generation on Z Double Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| YDTIE | Enable interrupt generation on Y Double Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| XDTIE | Enable interrupt generation on X Double Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| AO\_STI | And/or combination of Single Tap Interrupt events.  0 : AND combination of interrupt events (default).  1 : OR combination of interrupt events |
| ZSTIE | Enable interrupt generation on Z Single Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| YSTIE | Enable interrupt generation on Y Single Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |
| XSTIE | Enable interrupt generation on X Single Tap event.  0 :Disable interrupt (default).  1 :Enable interrupt |

* 1. FIFO\_CTRL Register (37h)

Fifo Operation Control

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | | 5 | 4 |  |  |  | 0 |
| FFC | | FMS[1:0] | | WTM\_TH[4:0] | | | | |

FIFO\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| FFC | 1: Fifo Clear(Fifo Buffer를 클리어함) 클리어 후 0으로 복귀.  0: None(default) |
| FMS[1:0] | FIFO Mode Selection  00: Bypass Mode (default).  01: FIFO Mode  10: Stream Mode  11: Stream-to-FIFO Mode(INT1에서 Interrupt가 발생 하면 Stream mode로 동작하다가  Fifo Mode로 동작)- Interrupt pin이 한 개이기 때문에 따로 Mapping 필요 없음. Interrupt pin이 2개가 되면 각각의 Pin에 동작 Mapping필요.. |
| WTM\_TH[4:0] | FIFO threshold. Watermark level setting.(0~31Level)  Default level:0 |

Fifo는 Low Power Mode에서는 비정상동작하므로, Low Power Mode에서 사용하지 말도록 App Note에 표기.

Fifo의 Read 및 Write

1. Burst Data Read시 –자동으로 Block모드로 바뀌어서 Burst Stop이 들어오면 Output Register로 Fifo에서 Update시킴.(Fifo를 사용할 때는 무조건 Burst로 억세스를 (권장)해야 정상적으로 Data를 가져갈 수 있다. Access 주소는 X축부터 Z축까지의 Output Register Address 범위로 제한한다 )
2. Single Read시 –

Block mode로 설정되어 있다면 X,Y,Z축중의 한 축의 두번째 (20h XH, 21h XL이라면 XL을 읽으면)Output Register를 읽는 상황이 완료되면 새로운 Data로 Fifo에서Output Register로 Update한다. 만약 첫번째만 계속 읽는다면 Block Mode이므로 업데이트가 되지 않는다.

None Block Mode- X,Y,Z축의 Output Register중의 MSB/LSB를 아무거나 읽으면 Fifo에서 한 개의 DataSet(X,Y,Z)를 output Register로 업데이트 한다.

1. Fifo가 Fifo Mode일 때 한 개가 비워지면 새로운 Data가 생성되는 ODR타임에 Fifo에 업데이트된다.

만약 Fifo모드일 때 연속적인 Data를 읽고 다시 또 읽고 연속적인 Data를 받고 싶은 경우 Fifo Clear를 하고 받거나 또는 Stream to Fifo를 사용한다.

1. Fifo Mode로 전환시는 Fifo Clear를 사용하고 사용해야 한다.
2. Bypass Mode일 때 Fifo 0 Address에 Data가 있다면 Output Register로 바로 읽어 놓도록 함.

그렇지 않으면 Low Power Mode(By Pass Fifo Mode)일 때 읽은 Data가 갱신되지 않고 같은 data만 나오는 현상 발생)//New data Ready Interrupt는 Low Power Mode일 때 읽어도 Clear가 되지 않음(clock이 없음) Normal로 와야 Clear됨.

* 1. FIFO\_DATA\_STATUS Register (38h)

This is the register that indicates FIFO stored data depth Level. It is a read only Register.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  | 5 | 4 |  |  |  | 0 |
| Reserved | | | FSD\_DEPTH[5:0] | | | | |

FIFO\_DATA\_STATUS Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| FSD\_DEPTH[5:0] | FIFO stored Data Depth Level |

* 1. INT\_FUNC\_CTRL1\_STATUS Register (39h)

NDR and WTM and FULL/EMPTY status of FIFO is indicated. It is a read only Register.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | | 6 | | 5 | | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | | Reserved | | Reserved | | NDR | FF\_WTM | FF\_FULL | FF\_EMPTY |

INT\_FUNC\_CTRL1\_STATUS Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| NDR | New Data Ready Interrupt Status  0:No Generated(default)  1:Generated Interrupt |
| FF\_WTM | Watermark status.  0 : FIFO filling is lower than WTM\_TH level(default)  1 : Generated WTM Interrupt (FIFO filling is equal or higher than WTM\_TH Level) |
| FF\_FULL | FIFO full status.  0 : FIFO not full(default)  1 : Generated FIFO full Interrupt |
| FF\_EMPTY | FIFO Empty status.  0 : FIFO not empty(default)  1 : Generated FIFO empty Interrupt |

**EVENT Duration**

High/Low/Tap/DTap등에서 25HZ~400HZ까지는 1/ODR의 시간에 의존하여 Duration이 내부적으로 측정에 사용되고 나머지ODR(700~ODRMax)는 4/ODR의 시간에 의존하여 내부적으로 사용된다.

Low Power Mode일 때는 Sleep+wakeup+샘플링 시간에 의존하여 Duration이 사용된다.

Duration이 0이면 Threshold만 넘는 샘플이 있다면 바로 Interrupt로 인식된다.

|  |  |  |  |
| --- | --- | --- | --- |
| **Duration Value** | **ODR** | **Normal Mode** | **Low Power Mode** |
| (0~255) | ≤400HZ | (Duration) \* (1/ODR) sec | (Duration)\*( Sleep+Wakeup+Sampling Time ) |
| >400Hz | (Duration) \* (4/ODR) sec |

Event 판정.

|  |  |  |  |
| --- | --- | --- | --- |
| **Event** | **Axis Configure** | **Measure** | **And Or** |
| Single Tap(And OR가 개별 존재) | X Select | X 축 Data 로만 판단. | 각 축간의 Event발생상황을 And /Or조건 확인하여 Interrupt발생 |
| Y Select | Y축 Data 로만 판단 |
| Z Select | Z축 Data 로만 판단. |
| Double Tap(And OR가 개별 존재) | X Select | X 축 Data 로만 판단. | 각 축간의 Event발생상황을 And /Or조건 확인하여 Interrupt발생 |
| Y Select | Y축 Data 로만 판단 |
| Z Select | Z축 Data 로만 판단 |
| High Motion(And Or가 Motion은 공용) | X Select | X 축 Data 로만 판단. | High/Low Motion을 동시에  And /Or조건 확인하여 Interrupt발생 |
| Y Select | Y축 Data 로만 판단 |
| Z Select | Z축 Data 로만 판단. |
| Low Motion(And Or가 Motion은 공용) | X Select | X 축 Data 로만 판단. |
| Y Select | Y축 Data 로만 판단 |
| Z Select | Z축 Data 로만 판단. |

* 1. MOTION\_CTRL Register (3Ah)

Motion Event Detection을 위한 설정 Control

S사의 Motion Detection 그림 무시. ( Duration에 의해 설정된 ODR기반의 시간.)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | MOTION\_DUR\_MODE | |

MOTION\_CTRL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| MOTION\_DUR\_MODE | 00:Up & down Duration (default).  01:Only Up Duration  10:Only down Duration  11: No Duration |

**아래 그림은 사용되지 않음.**

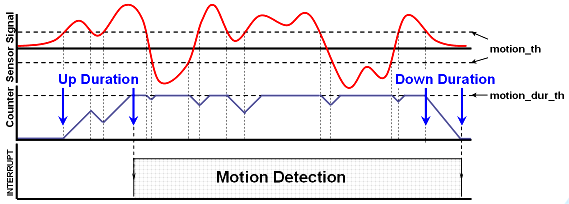


Figure 13. Motion Detection Diagram

* 1. MOTION\_STATUS Register (3Bh)

Motion Interrupt의 발생 Status정보 표시.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ZH | YH | XH | Reserved | ZL | YL | XL |

MOTION\_STATUS Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| ZH | Z High Event.  0 : no interrupt(default)  1 : ZH Interrupts has occurred |
| YH | Y High Event.  0 : no interrupt(default)  1 : YH Interrupts has occurred |
| XH | X High Event.  0 : no interrupt(default)  1 : XH Interrupts has occurred |
| ZL | Z Low Event.  0 : no interrupt(default)  1 : ZL Interrupts has occurred |
| YL | Y Low Event.  0 : no interrupt(default)  1 : YL Interrupts has occurred |
| XL | X Low Event.  0 : no interrupt(default)  1 : XL Interrupts has occurred |

* 1. MOTION\_HIGH\_TH Register (3Ch)

Motion Detection시의 High Event의 Threshold 설정.(Direction모드에 따라 적용방법이 달라짐 ST의 Appnote 동작모드 참조)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| HIGH\_TH[7:0] | | | | | | | |

MOTION\_HIGH\_TH Register(R/W)

Initial value: 0xBE

|  |  |
| --- | --- |
| **Name** | **Description** |
| HIGH\_TH[7:0] | High Detection Threshold. Unsigned format  Sensor Signal Data> HIGH\_TH(=High Event Detection)  Scale Factor: x128  Default : 0xBE (190\*128= 24320 accel\_data Count)  High Detection  Direction Mode: accel\_data (COUNT)>HIGH\_TH  No Direction Mode: ABS( accel\_data(COUNT)) >HIGH\_TH |

* 1. MOTION\_HIGH\_DUR Register (3Dh)

Motion Detection시의 High Event의 Duration설정

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| HIGH\_DUR [7:0] | | | | | | | |

MOTION\_HIGH\_DUR Register(R/W)

Initial value: 0x02

|  |  |
| --- | --- |
| **Name** | **Description** |
| HIGH\_DUR | High Event Duration Threshold. Unsigned format.  Default:0x02(40msec) -> (default ODR 50hZ) |

* 1. MOTION\_LOW\_TH Register (3Eh)

Motion Detection시의 Low Event의 Threshold 설정.(Direction모드에 따라 적용방법이 달라짐 ST의 Appnote 동작모드 참조)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| LOW\_TH[7:0] | | | | | | | |

MOTION\_LOW\_TH Register(R/W)

Initial value: 0x2D

|  |  |
| --- | --- |
| **Name** | **Description** |
| LOW\_TH[7:0] | Low Event Detection Threshold. Unsigned format.  Sensor Signal Data <LEVENT\_TH(= Low Event Detection)  Scale Factor: x128  Default: 0x2D (45\*128=5760 accel\_data Count)  Low Event Detection  Direction Mode: accel\_data(COUNT) < -LOW\_TH(내부적으로–부호로 처리)  No Direction Mode: ABS(accel\_data(COUNT)) )<LOW\_TH |

* 1. MOTION\_LOW\_DUR Register (3Fh)

Motion Detection시의 Low Event의 Duration설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| LOW\_DUR [7:0] | | | | | | | |

MOTION\_LOW\_DUR Register(R/W)

Initial value: 0x02

|  |  |
| --- | --- |
| **Name** | **Description** |
| LOW\_DUR | Low Event Duration Threshold. Unsigned format.  Default:0x02(40msec) -> (default ODR 50hZ) |

* 1. TAP\_INT\_STATUS Register (40h)

Tap/DTap Interrupt의 발생 Status정보 표시.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ZDT | YDT | XDT | Reserved | ZST | YST | XST |

TAP\_INT\_STATUS Register(R/O)

Initial value: -

|  |  |
| --- | --- |
| **Name** | **Description** |
| ZDT | Z Double Tap.  0 : no interrupt(default)  1 : ZDT Interrupt has occurred |
| YDT | Y Double Tap.  0 : no interrupt(default)  1 : YDT Interrupt has occurred |
| XDT | X Double Tap.  0 : no interrupt(default)  1 : XDT Interrupt has occurred |
| ZST | Z Single Tap.  0 : no interrupt(default)  1 : ZST Interrupt has occurred |
| YST | Y Single Tap.  0 : no interrupt(default)  1 : YST Interrupt has occurred |
| XST | X Single Tap.  0 : no interrupt(default)  1 : XST Interrupt has occurred |

* 1. TAP\_TH Register (41h)

Tap Detection시의 threshold값 설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| TAP\_TH[7:0] | | | | | | | |

TAP\_TH Register(R/W)

Initial value: 0x40

|  |  |
| --- | --- |
| **Name** | **Description** |
| TAP\_TH[7:0] | Tap Detection Threshold. Unsigned format.  Sensor Signal Data>TAP\_TH (=Tap Detection)  Scale factor : x128(0~32768)  Default: 0x40 ( 64\*128배= 8192 Accel data count)  Tap Detection(Direction Mode설정 비트와는 상관없다)  Abs(Accel data(COUNT))>TAP\_TH |

* 1. TAP\_DUR Register (42h)

Tap Detection시의 Duration 설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| TAP\_DUR [7:0] | | | | | | | |

TAP\_DUR Register(R/W)

Initial value: 0x07

|  |  |
| --- | --- |
| Name | Description |
| TAP\_DUR | Tap Detection Threshold. Unsigned format.  Sensor Signal Duration <TAP\_DUR (=Tap Detection)  Default:0x07(140msec) -> (default ODR 50hZ)  Tap Event Detection  Sensor Signal Duration <TAP\_DUR (time\_lmt\_th-삼성그림) |

* 1. DTAP\_TIMEWINDOW\_DUR Register (43h)

Double Tap Detection을 위한 첫 번째 Tap이후의 Time Window Duration

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DTAP\_TIMEWND\_DUR [7:0] | | | | | | | |

DTAP\_TIMEWINDOW\_DUR Register(R/W)

Initial value: 0x28

|  |  |
| --- | --- |
| **Name** | **Description** |
| DTAP\_TIMEWIND\_DUR | Double Tap Time Window Threshold. Unsigned format.  Second Tap detection Time Window Duration after first tap detection  Tap Detection< DTAP\_TIMEWIND\_DUR (=double Tap Detection)  Default:0x28 (800msec)-- >(default ODR 50hZ)  double Tap Detection. |

* 1. TAP\_LATENCY\_DUR Register (44h)

Tap후 지연 시간 동안 다른 입력무시

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| TAP\_LATENCY\_DUR [7:0] | | | | | | | |

TAP\_LATENCY\_DUR Register(R/W)

Initial value: 0x05

|  |  |
| --- | --- |
| **Name** | **Description** |
| TAP\_LATENCY\_DUR | Tap Latency Duration Threshold. Unsigned format.  Ignore additional events after First Tap  Default: 0x05(100msec) - >(default ODR 50hZ) |

입력무시가 끝난 후 상태가 Data가 Threashold이상이면 그때부터 Tap\_Duration을 Count하여 측정에 포함시킨다.

그림을 다시 그릴필요가 있음

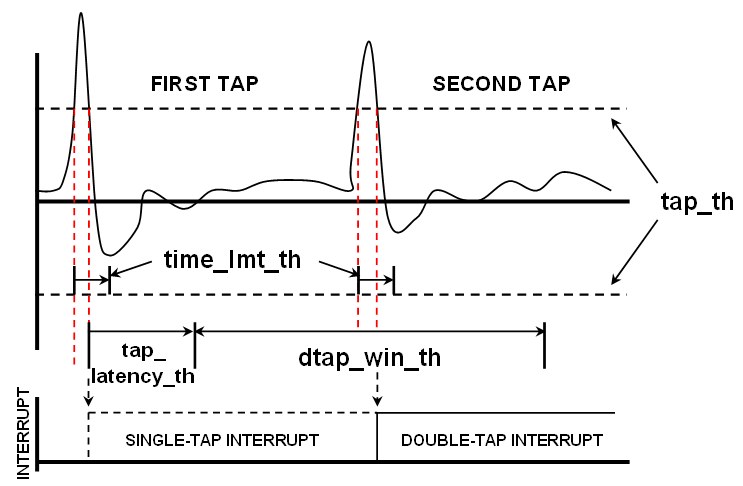


Figure 14. Tap Event Diagram

* 1. AFE\_WT\_MODE Register (4Ch)

AFE Wafer Level Test시 CLKO로 출력되는 signal을 설정.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | |  | |  | |  | | 1 | | 0 |
| reserved | reserved | | reserved | | reserved | | reserved | | reserved | | T\_MODE [1:0] | |

AFE\_WT\_MODE Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| T\_MODE[1:0] | Default: 00  00 : VOP\_T = VCOM, VON\_T = VCOM\_ADC, CLKO = GND  01 : VOP\_T = CVOP, VON\_T = CVON, CLKO = CLK25KHZ  10 : VOP\_T = PGOP, VON\_T = PGON, CLKO = CLKO25K  11 : VOP\_T = AOUTP, VON\_T = AOUTN, CLKO = CLK1P6M |

* 1. CMI CTRL Register (4Dh)

Main Bias Control.(높이면 성능은 좋아지지만 Current와 문제가 생길 수 있음)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | | 4 | | 3 | |  |  | 0 |
| Reserved | Reserved | | Reserved | | Reserved | | CMI [3:0] | | | |

CMI CTRL Register(R/W)

Initial value: 0x04

|  |  |
| --- | --- |
| **Name** | **Description** |
| CMI[3:0] | Default:0x04  0000  …  0100: 300uA  …  1111:  Bit Definition |

OTP 블록의 Register는 Bank에 쓸 때 Bit할당이 안되어 있는 Bit들은 모두 0로 써줘야 Loading시 문제가 생기지 않는다.

* 1. TEST\_DREGISTER Register(4Eh)

Digital test for Bist Test

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  | |  | |  | | 0 | |
| Reserved | Reserved | | Reserved | | Reserved | | Reserved | | Reserved | | Reserved | | D\_REG |

TEST\_DREGISTER Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| D\_REG | Digital Test for Register file. Default: 0  0: Diable Bist Test  1: Start Bist Test |

* 1. TEST\_DREGISTER\_STATUS Register (4Fh)

Digital test result status flag for Bist.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  | |  | | 1 | | 0 |
| Reserved | Reserved | | Reserved | | Reserved | | Reserved | | Reserved | | D\_REG\_STAT | |

TEST\_DREGISTER Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| D\_REG\_STAT[1] | Status flag of Bist Test Result  1: Fail  0:Pass |
| D\_REG\_STAT[0] | Status flag for Bist  0: No Test  1: Bist Test Complete |

* 1. CP\_OT\_PX Register (50h)

X축의 Positive방향의 Capacitor offset Trimming을 위한 Level설정

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_PX [4:0] | | | | |

CP\_OT\_PX Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_PX[4:0] | X축의 Positive방향의 Capacitor Offset Trimming level  0: 0fF(default)  1: 10fF  …  11111: 310fF |

* 1. CP\_OT\_NX Register (51h)

X축의 Negative방향의 Capacitor offset Trimming을 위한 Level설정

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_NX [4:0] | | | | |

CP\_OT\_NX Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_NX[4:0] | X축의 Negative방향의 Capacitor Offset Trimming level  0: 0fF (default)  1: 10fF  …  11111: 310fF |

* 1. CP\_OT\_PY Register (52h)

Y축의 Positive방향의 Capacitor offset Trimming을 위한 Level설정

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_PY [4:0] | | | | |

CP\_OT\_PY Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_PY[4:0] | Y축의 Positive방향의 Capacitor Offset Trimming level  0: 0fF(default)  1: 10fF  …  11111: 310fF |

* 1. CP\_OT\_NY Register (53h)

Y축의 Negative방향의 Capacitor offset Trimming을 위한 Level설정

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_NY [4:0] | | | | |

CP\_OT\_NY Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_NY[4:0] | Y축의 Negative방향의 Capacitor Offset Trimming level  0: 0fF (default)  1: 10fF  …  11111: 310fF |

* 1. CP\_OT\_PZ Register (54h)

Z축의 Positive방향의 Capacitor offset Trimming을 위한 Level설정.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_PZ [4:0] | | | | |

CP\_OT\_PZ Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_PZ[4:0] | Z축의 Positive방향의 Capacitor Offset Trimming level  0: 0fF(default)  1: 10fF  …  11111: 310fF |

* 1. CP\_OT\_NZ Register (55h)

Z축의 Negative방향의 Capacitor offset Trimming을 위한 Level설정.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| Reserved | Reserved | | Reserved | | CP\_OT\_NZ [4:0] | | | | |

CP\_OT\_NZ Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| CP\_OT\_NZ[4:0] | Z축의 Negative방향의 Capacitor Offset Trimming level  0: 0fF (default)  1: 10fF  …  11111: 310fF |

* 1. PGA \_GT\_XY Register (56h)

**PGA\_Mode가 2fF Mode일 때는 Gain의 Min(5)~Max(11.25)이고 default은 7.5이다 -> (12+GainValue)/2.4**

X/Y축의 Sensitivity Trimming을 위해 PGA Gain을 Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  | 3 |  |  | 0 |
| PGA \_GT\_X [3:0] | | | | PGA \_GT\_Y [3:0] | | | |

PGA \_GT\_XY Register(R/W)

Initial value: 0x66

|  |  |
| --- | --- |
| **Name** | **Description** |
| PGA \_GT\_X[3:0] | Analog PGA Gain을 설정.  Default :0110(x3)->((12+PGA\_GT\_X)/6)  0: x2  …  1111: x4.5 |
| PGA \_GT\_Y[3:0] | Analog PGA Gain을 설정.  Default :0110(x3)->((12+ PGA\_GT \_Y)/6)  0: x2  …  1111: x4.5 |

* 1. PGA \_GT\_Z Register (57h)

Z축의 Sensitivity Trimming을 위해 PGA Gain을 Control

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | 4 | 3 | 2 | 1 | 0 |
| PGA \_GT\_Z [3:0] | | | | Reserved | Reserved | Reserved | PGA\_MODE |

PGA \_GT\_Z Register(R/W)

Initial value: 0x60

|  |  |
| --- | --- |
| **Name** | **Description** |
| PGA \_GT\_Z[3:0] | Analog PGA Gain을 설정.  Default :0110(x3)->((12+ PGA\_GT \_Z)/6)  0: x2  …  1111: x4.5 |
| PGA\_MODE | PGA Gain Mode를 선택. (OTP에 결합된 MEMS에 따라 저장되어야 함)  0: 5fF Mode(default)  1: 2fF Mode |

* 1. TOSC3 & VBGR Register (58h)

OSC1 temperature compensation, 0.9V BOT Temperature compensation(band gap reference trimming)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  | 3 |  |  | 0 |
| TOSC3 [3:0] | | | | VBGR[3:0] | | | |

TOSC3&VBGR Register(R/W)

Initial value:0x78

|  |  |
| --- | --- |
| **Name** | **Description** |
| TOSC3[3:0] | OSC1 Temp. Compensation  Default: 0111 |
| VBGR[3:0] | Band gap reference trimming  Default: 1000 1.2V  0000: ??  …  …  1000: 1.2V  …  ….  1111: ?? |

* 1. DVP Register (59h)

DVP : 0.9V Reference Trimming (default : 10000)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  | | 4 | |  |  |  | 0 |
| reserved | reserved | | reserved | | DVP[4:0] | | | | |

DVP Register (R/W)

Initial value: 0x10

|  |  |
| --- | --- |
| **Name** | **Description** |
| DVP[4:0] | 0.9V Reference trimming ratio selection  Default: 10000  00000: 1.136(0.789V~0.795V)  …  10000: 1 (0.897V->0.903V)  …  11111: 1.899(0.999V~1.005V) |

* 1. TSEN\_DC Register (5Ah)

Temperature DC Offset Trimming을 수행.

DC : 0.9V@25℃

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| TSEN\_DC[7:0] | | | | | | | |

TSEN\_DC Register (R/W)

Initial value: 0x02-23도를 00으로 맞춰야 하니 2의 오프셋을 기본값으로 가짐.

|  |  |
| --- | --- |
| **Name** | **Description** |
| TSEN\_DC[7:0] | Temperature DC Offset Trimming (2’s compliment)  Default: 0x02=(23C) |

* 1. TOSC1 Register (5Bh)

1.6Mhz Oscillator Clock Trimming을 수행.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 |  |  |  |  |  | 0 |
| reserved | TOSC1[6:0] | | | | | | |

TOSC1 Register (R/W)

Initial value: 0x3F

|  |  |
| --- | --- |
| **Name** | **Description** |
| TOSC1[6:0] | 1.6Mhz OSC1 trimming ratio selection  Default: 0111111  0000000: 1.4035(1.133Mhz~1.142Mhz)  …  0111111: 1(1.595Mhz~1.603Mhz)  …  1111111: 0.592 (2.687Mhz~2.719Mhz) |

* 1. TOSC2 Register (5Ch)

25khz Oscillator Clock Trimming을 수행.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | |  |  |  |  | 0 |
| reserved | reserved | | TOSC2[5:0] | | | | | |

TOSC2 Register (R/W)

Initial value: 0x1F

|  |  |
| --- | --- |
| **Name** | **Description** |
| TOSC2[5:0] | 25khz OSC2 trimming ratio selection  Default:011111 - 25Khz  000000: 0.535(46.10khz~47.50khz)  …  011111: 1(24.61khz~25.10khz)  …  111111: 1.495(16.60khz~16.81khz) |

* 1. DFACT\_GT\_X Register (5Dh)

X축의 Sensitivity를 Fine Tuning하기 위해 Digital Gain 조절 (x0~x4).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT\_GT\_X [7:0] | | | | | | | |

DFACT\_GT\_X Register(R/W)

Initial value: 0x40

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_GT\_X[7:0] | Digital Gain을 0(x0) ~0xff(x3.98)배까지 4배의 Fine Control :  Default:0x40(1배) |

* 1. DFACT\_GT\_Y Register (5Eh)

Y축의 Sensitivity를 Fine Tuning하기 위해 Digital Gain 조절(x0~x4).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT\_GT\_Y [7:0] | | | | | | | |

DFACT\_GT\_Y Register(R/W)

Initial value: 0x40

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_GT\_Y[7:0] | Digital Gain을 0(x0) ~0xff(x3.98)배까지 4배의 Fine Control  Default:0x40( 1배) |

* 1. DFACT\_GT\_Z Register (5Fh)

Z축의 Sensitivity를 Fine Tuning하기 위해 Digital Gain 조절 (x0~x4).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT\_GT\_Z [7:0] | | | | | | | |

DFACT\_GT\_Z Register(R/W)

Initial value: 0x40

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_GT\_Z[7:0] | Digital Gain을 0(x0) ~0xff(x3.98)배까지 4배의 Fine Control  Default:0x40(1배) |

* 1. DFACT\_OFS\_XYZ Register (60h)

Digital Factory Offset Control의 X/Y/Z 축 Positive/Negative Direction을 설정.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  | 3 | 2 | 1 | 0 |
| Reserved | | | | | FACT\_ZOS | FACT\_YOS | FACT\_XOS |

DFACT\_OFS\_XYZ Register(R/W)

Initial value: 0x07

|  |  |
| --- | --- |
| **Name** | **Description** |
| FACT\_ZOS | Digital Z Offset fine tuning을 위한 Positive/Negative 적용을 선택  1: Positive Direction (default).  0: Negative Direction |
| FACT\_YOS | Digital Y Offset fine tuning을 위한 Positive/Negative 적용을 선택  1: Positive Direction (default).  0: Negative Direction |
| FACT\_XOS | Digital X Offset fine tuning을 위한 Positive/Negative 적용을 선택  1: Positive Direction (default).  0: Negative Direction |

* 1. DFACT\_OT\_X Register (61h)

X축의 Offset을 Fine Tuning하기 위해 Digital Offset을 조절 (±0~16384COUNT).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT\_OT\_X [7:0] | | | | | | | |

DFACT\_OT\_X Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_OT\_X[7:0] | Digital Offset을± 0~16384COUNT까지 Control  FACT\_XOS bit에 의해 positive/negative적용.  Default:0x00 (0)  Scale:x64 |

* 1. DFACT\_OT\_Y Register (62h)

Y축의 Offset을 Fine Tuning하기 위해 Offset을 조절 (±0~16384COUNT).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT\_OT\_Y [7:0] | | | | | | | |

DFACT\_OT\_Y Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_OT\_Y[7:0] | Digital Offset을± 0~16384COUNT까지 Control  FACT\_YOS bit에 의해 positive/negative적용.  Default:0x00(0)  Scale:x64 |

* 1. DFACT \_OT\_Z Register (63h)

Z축의 Offset을 Fine Tuning하기 위해 Offset을 조절 (±0~16384COUNT).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  |  |  |  | 0 |
| DFACT \_OT\_Z [7:0] | | | | | | | |

DFACT\_OT\_Z Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| DFACT\_OT\_Z[7:0] | Digital Offset을± 0~16384COUNT까지 Control  FACT\_ZOS bit에 의해 positive/negative적용  Default:0x00(0)  Scale:x64 |

* 1. DSIGN\_CONTROL Register (64h)

각 축의 Acceleration Signal 출력방향을 Control

//Low Pass Filter 전 에서 Factory Gain과 Offset 처리 후에 Sign을 출력방향을 처리하고 User Offset/Gain을 처리한다.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 |  |  |  | 3 | 2 | 1 | 0 |
| Reserved | | | | | ACC\_ZSIGN | ACC\_YSIGN | ACC\_XSIGN |

DSIGN\_CONTROL Register(R/W)

Initial value: 0x00

|  |  |
| --- | --- |
| **Name** | **Description** |
| ACC\_ZSIGN | Controls Z- Axis signal output  1: Reverse –출력방향을 뒤집는다.  0: Bypass(default) 그대로 출력 |
| ACC\_YSIGN | Controls Y- Axis signal output  1:Reverse 출력방향을 뒤집는다.  0:Bypass(default) 그대로 출력 |
| ACC\_XSIGN | Controls X- Axis signal output  1:Reverse 출력방향을 뒤집는다.  0:Bypass(default) 그대로 출력 |

* 1. OTP\_PM Register (65h)

OTP Power Mode Control

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | | 5 | | 4 | | | 3 | 2 | 1 | 0 |
| Reserved | | Reserved | | Reserved | | Reserved | Reserved | | Reserved | Reserved | OTP\_PM |

OTP\_PM Register(R/W)

Initial value: 0x01

|  |  |
| --- | --- |
| **Name** | **Description** |
| OTP\_PM | Booting시 Loading후 OTP의 전원상태를 설정한다.  1:Power ON(default)-Normal  0:Power Down |

**OTP Power control은 현재 Register에 적용되면 Power가 바로 On/Off되어 OTP에 Writing이 불가능해지므로, 이 Register는 직접 0으로 설정하지 않고 Power On상태로 OTP에 쓰고 해당 Bank에 매뉴얼로 65h에 해당하는 15h Address를 직접 0으로 써주고, Rebooting시 자동으로 적용되도록한다.**

* 1. OFFSET\_DATA\_MSB Register(70h)

Offset Data MSB Value.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFFSET\_DATA\_MSB[7:0] | | | | | | | |

OFFSET\_DATA\_MSB Register(R)

Initial value:

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFFSET\_DATA\_MSB]7:0] | Offset data MSB status. |

* 1. OFFSET\_DATA\_LSB Register(71h)

Offset Data LSB Value.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFFSET\_DATA\_LSB[7:0] | | | | | | | |

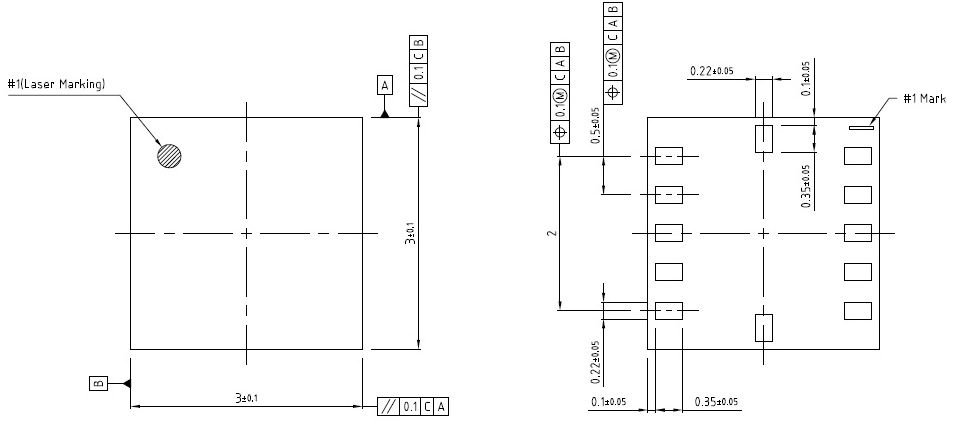
OFFSET\_DATA\_LSB Register(R)

Initial value:

|  |  |
| --- | --- |
| **Name** | **Description** |
| OFFSET\_DATA\_LSB]7:0] | Offset data LSB status. |

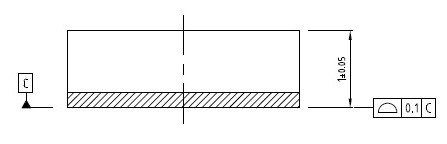
1. Package Information
   1. Package dimensions

SGA100 is packaged in a 3mm x 3mm x 1.0mm 12LGA Package.



Bottom View

Top View



Side View

Figure 15. Top, Bottom and Side views of the LGA Package (Dimensions in mm)

* 1. Axes orientation

The Following diagram describes the orientation of the package with respect to the axes of

acceleration measurement.

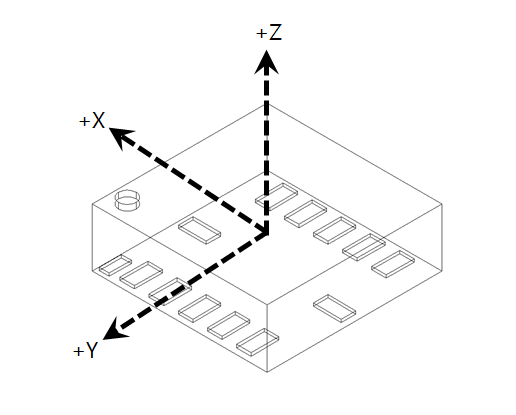
****

Figure 16. Axis Orientation of the SGA100

1. Revision History

|  |  |  |
| --- | --- | --- |
| **Revision** | **Date** | **changes** |
| 1.0 |  | First Release |